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ELEKTOR PUBLISHERS LTD. 6, Stour Street, Canterbury, CT1 2XZ, Tel.: 0227-54430.
The popularity of television tennis games has prompted Elektor to produce a design that can easily be built by the home constructor for a modest cost. Although several designs have previously appeared on the market, it was felt that there was a need for a simple circuit using a minimum of components.

In order to keep costs down the TV tennis circuit generates the most basic 'picture' possible, i.e. two 'bats' and a 'ball'. The ball is 'served' from one side of the screen or the other and the players move their bats up and down the screen to intercept the path of the ball. If the ball strikes a bat it is returned, otherwise it leaves the side of the screen and a 'new ball' must be served. Should the ball reach the upper or lower edge of the screen during its traverse across the screen it will 'bounce'. The upper and lower boundaries are, however, not displayed on the screen.

The output of the TV tennis game is used to modulate a VHF oscillator so that the game may be plugged direct into the aerial socket of a television.

Principle of operation
For those not familiar with TV a brief resume of the principles involved may prove helpful. A TV picture is, of course, generated by an electron beam scanning across the phosphor-coated face of a cathode-ray tube in a zig-zag fashion from top to bottom. At the end of each horizontal line the beam flies back to the left hand edge of the screen and starts the next line slightly lower down the screen. Each complete scan (frame) of the picture consists of either 405 or 625 lines, depending on the transmission standard. To reduce the bandwidth required to transmit the video information a complete frame is not transmitted in a single scanning of the picture, but is made up of two 'fields' containing half the number of lines in a frame. These two fields are interlaced with each other to make up a complete frame. Fields are transmitted at a 50 Hz rate, therefore frames are transmitted at half that rate, i.e. 25 frames per second.

The video waveform
In order to build up a picture on the screen the brightness of the trace must be modulated by varying the electron
beam current. This is controlled by the amplitude of the video waveform. So that the scanning of the electron beam in the TV set is in synchronism with the received signal in order to build up the picture correctly, field sync. pulses are transmitted (at the end of each field) and line sync. pulses are transmitted (at the end of each line).

To distinguish sync. pulses from video information, sync. pulses are negative-going and confined to a voltage below that required for zero beam current (black level). Video information occupies a range of voltages above black level up to the voltage required to saturate the TV tube phosphor (peak white level). Circuitry in the TV distinguishes between sync. pulses and video information. Field sync. pulses also have a longer duration to distinguish them from line sync. pulses. From the foregoing some of the requirements for the circuit become apparent. Firstly, the circuit must contain oscillators capable of generating field and sync. pulses at the appropriate frequencies (50 Hz and 15625 Hz respectively). Secondly, circuitry for generating the bat and ball waveforms, and for controlling the movement of these, is required. Fortunately, since we are concerned only with white bats and ball on a black background the only modulation required is peak white level or black level, so analogue circuitry is not needed to produce these waveforms, and digital logic circuits can be used to generate the rectangular pulses necessary.

The operation of the circuit is best understood with the aid of a block diagram (figure 1). Sync. pulses from the field and line oscillators are mixed in the video mixer and then fed to the modulator. They are also used to control the timing of the other waveforms.

Block Diagram

The operation of the circuit is best understood with the aid of a block diagram (figure 1). Sync. pulses from the field and line oscillators are mixed in the video mixer and then fed to the modulator. They are also used to control the timing of the other waveforms.

All the video waveforms are generated using monostable multivibrators and in the generation of the 'bats' is simple this will be considered first. The left hand player's horizontal bat generator IC5 is triggered continuously from the line sync. oscillator. A presettable trigger delay is incorporated so that the pulse appears a little time after the line sync. pulse. This ensures that the bat appears some way in from the left hand edge of
screen. The right-hand player's horizontal generator IC3 incorporates a delay so that this bat appears at the right-hand edge of the screen. Since the triggering occurs after every sync pulse the result would be a vertical band of white the full height of the screen. This is where the vertical bat generator (IC6 left, IC4 right) comes in. This monostable is triggered from the vertical sync pulses via a delay which is continuously variable by the player, and determines the vertical position of the bat. The delayed pulse from the vertical bat generator gates the pulses from the horizontal oscillator so that they are allowed through for the duration of this pulse. The result is thus a vertical bar on the screen whose vertical position can be varied by the player and whose height (length of the bat) is determined by the duration of the vertical pulse. The same applies for both left- and right-hand bats.

The ball is generated in a similar manner with two monostables (IC1 and IC2). However, since the ball is continuously moving this in effect means that for movement to the right the horizontal delay is increasing all the time, for movement to the left it is decreasing.

Downwards movement the vertical delay is increasing, while for upwards movement it is decreasing. Of course it is necessary to reverse the direction of ball travel when the ball bounces off a bat or the upper and lower boundaries. This part of the circuit operates as follows:

The horizontal ball pulse generator (1) is triggered via a delay by the line sync pulses. The delay, and therefore the horizontal position of the ball on the screen, is controlled by the output of a ramp which varies the trigger delay linearly. The slope of the ramp (positive-going, negative-going) and hence the direction of ball travel is determined by the state of flip-flop FF2. If FF2 is set the ball will travel to the right. If the ball does not strike a bat it will leave the side of the screen and will not return until it is ‘served’, since the state of the flip-flop is not changed and the integrator output will eventually saturate in one direction or another. Service will be dealt with in the description of the full circuit.

Travel of the ball in the vertical direction is controlled in a similar fashion, but here the change of direction occurs at the upper and lower boundaries. The lower border of the picture corresponds with the leading (negative-going) edge of the field sync pulse, so change of direction at this boundary is accomplished by gates the ball signal with the field sync pulse in N5. To change ball direction at the top of the picture a monostable (IC9) is triggered by the trailing edge of the field sync pulse. The output pulse of the monostable is gated with the ‘ball’ signal to reset FF1. A timing diagram showing how the various pulses are gated together to produce the bat and ball display is given in figure 2a, together with the general appearance of the complete waveform as seen on an oscilloscope.

Complete Circuit
The complete circuit is given in figure 3. Field sync pulses are produced by the astable multivibrator driving a monostable to produce pulses of the correct length. Box B contains similar circuitry, but operating at a much higher frequency, to produce line sync pulses. The Q outputs of these monostables (to produce the negative-going sync pulses) are fed via D3 and D4

Figure 1. Block diagram of TV Tennis game (excluding modulator/oscillator).

Figure 2a. The horizontal and vertical waveforms are gated together as shown to produce the bat and ball display.

Figure 2b. The complete video waveform as seen on an oscilloscope.
figure 3. The complete circuit of the TV Tennis game. The modulator/oscillator circuit is shown inset at the bottom right-hand corner.

figure 3a. Suggested modification to derive old sync pulses from the mains for mains-only versions of the game. This should give a more stable picture than the free-running oscillator.

figure 4. Circuit of the mains power supply for TV Tennis.

Parts list for figures 3, 5 and 7

Resistors:
- \( R3, R4, R47 = 33k \)
- \( R1, R2, R39, R43, R55 = 4.7k \)
- \( R13, R16, R17, R20, R21, R24, R25, R8, R12 = 4.7k \)
- \( R7, R11 = 10k \)
- \( R14, R18, R22, R6, R30, R34, R40, R44, R57 = 100k \)
- \( R15, R19, R23, R27, R31, R35, R53 = 2k2 \)
- \( R37, R41, R48, R52 = 2.7k \)
- \( R38, R42 = 10\Omega \)
- \( R45 = 1k8 \)
- \( R46, R49, R54 = 1k \)
- \( R50 = 12\Omega \)
- \( R61 = 470\Omega \)
- \( R68 = 27k \)
- \( P1, P2 = 4k7 \) lin. preset
- \( P3, P6 = 47k \) lin.
- \( P4, P5, P7, P8 = 100k \) lin. preset

Capacitors:
- \( C5, C6 = 15n \)
- \( C3 = 22n \)
- \( C4, C8, C11, C14, C17, C20, C23 = 100n \)
- \( C5, C6 = 15n \)
- \( C7 = 390p \)
- \( C9, C15, C21 = 1n5 \)
- \( C10, C16, C22 = 180p \)
- \( C12, C18, C24, C26, C27, C28, C29, C47 = 470n \)
- \( C13 = 68n \)
- \( C19, C25, C30 = 220n \)
- \( C31, C32 = 47\mu F, 10V \)
- \( C33 = 3n3 \)
- \( C34 = 150n \)
- \( C35 = 3p3 \)
- \( C36 = 4...20p \) trimmer
- \( C37 = 47p \)

Semiconductors:
- \( T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11, T12 = BC347B \)
- \( T13 = AF239 \)
- \( D1 ... D14 = 1N4148 \)
- \( IC1, IC2, IC3, IC4, IC5, IC6, IC7, IC8, IC9 \)
- \( IC10 = 74121 \)
- \( IC10, IC11 = 74140 \)
- \( IC12 = 7402 \)
- \( IC13 = 7474 \)

Sundries:
- \( L = 4\) wdg, \( 1mm \) \( \phi \) Cu, \( \phi 8 \) mm
- \( HF Tr = 100\Omega \rightarrow 240\Omega \) impedance converter (see text)

* see text

Parts list for figures 3, 5 and 7

Resistors:
- \( R3, R4, R47 = 33k \)
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- \( R13, R16, R17, R20, R21, R24, R25, R8, R12 = 4.7k \)
- \( R7, R11 = 10k \)
- \( R14, R18, R22, R6, R30, R34, R40, R44, R57 = 100k \)
- \( R15, R19, R23, R27, R31, R35, R53 = 2k2 \)
- \( R37, R41, R48, R52 = 2.7k \)
- \( R38, R42 = 10\Omega \)
- \( R45 = 1k8 \)
- \( R46, R49, R54 = 1k \)
- \( R50 = 12\Omega \)
- \( R61 = 470\Omega \)
- \( R68 = 27k \)
- \( P1, P2 = 4k7 \) lin. preset
- \( P3, P6 = 47k \) lin.
- \( P4, P5, P7, P8 = 100k \) lin. preset

Capacitors:
- \( C5, C6 = 15n \)
- \( C3 = 22n \)
- \( C4, C8, C11, C14, C17, C20, C23 = 100n \)
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- \( C10, C16, C22 = 180p \)
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- \( C19, C25, C30 = 220n \)
- \( C31, C32 = 47\mu F, 10V \)
- \( C33 = 3n3 \)
- \( C34 = 150n \)
- \( C35 = 3p3 \)
- \( C36 = 4...20p \) trimmer
- \( C37 = 47p \)

Semiconductors:
- \( T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11, T12 = BC347B \)
- \( T13 = AF239 \)
- \( D1 ... D14 = 1N4148 \)
- \( IC1, IC2, IC3, IC4, IC5, IC6, IC7, IC8, IC9 \)
- \( IC10 = 74121 \)
- \( IC10, IC11 = 74140 \)
- \( IC12 = 7402 \)
- \( IC13 = 7474 \)

Sundries:
- \( L = 4\) wdg, \( 1mm \) \( \phi \) Cu, \( \phi 8 \) mm
- \( HF Tr = 100\Omega \rightarrow 240\Omega \) impedance converter (see text)

Parts list for figures 3, 5 and 7

To the junction of R58 and R59. This portion of the circuitry functions as the video mixer. Black level occurs when the Q outputs of IC7 and IC8 are both high and the bat and ball inputs to D11, D12 and D13 are all low. The voltage at the junction of R58 and R59 is then solely determined by the value of these resistors and is about 1.35 V. When a sync pulse occurs then the junction of these two resistors is held down to about 1 V via D3 or D4. When bat or ball signals occur the inputs to D11, D12 or D13 go high, so the potential at the junction of R58 and R59 becomes about 4 V. If the unit is to be used for mains only operation the astable in box A can be dispensed with and field sync pulses may be derived from the 50 Hz mains by the modification shown in figure 3a. P1, R5, R6, C1 and C2 are omitted; the sync pulses are fed in at the original connection to the positive side of C1 on the board, and the track between this point and the output of N2 (pin 6 of IC10) must be broken.

The sync pulses are buffered by emitter followers T1 and T2 to avoid loading the monostables excessively. The buffered sync pulses are then fed via the trigger delays to the appropriate monostables which generate the horizontal and vertical components of the ball and bat waveforms. The trigger delay circuits are all identical in principle and merely vary in component values. The trigger delay for IC3 operates as follows: normally T5 is turned on by base current through R23. Its collector voltage (and hence the A in the block diagram have been replaced by NOR-gates connected to the Q outputs of the monostables. This is of course exactly equivalent to AND-gates connected to the Q outputs (De Morgan's theorem).

The horizontal bat trigger delays are preset, by P7 for the right-hand player, and by P4 for the left-hand player. This allows the position of the bats to be adjusted to a few cm away from the sides of the screen. The vertical position of the bats is continuously adjustable, by P6 for the right-hand player and P3 for the left-hand player. P5 and P8 are presets used to adjust the bat position...
so that P6 and P3 are effective over the full height of the screen.

Service of the ball

It is evident that if the state of FF2 is not reversed by a coincidence between the ball and one of the bat signals then the voltage at the emitter of T12 will continue to rise or fall as C32 either charges or discharges, until it reaches either zero volts or supply minus the base-emitter voltage of T12. The ball will then disappear off one side of the screen or the other and will not return. For this reason (as well as for the rules of the game) it is necessary to 'serve' the ball when this has occurred.

Ideally the ball should emanate from the bat of the player who is serving. However, in practice this is difficult to achieve as it means that at the instant of service the vertical ball trigger delay must be matched to the vertical bat trigger delay. Since the delay circuits are independent component tolerances will make this unlikely. It is, however, possible to make the ball service dependent upon the bat position at the time of service, though not coincident with it.

Service is accomplished as follows: for a service by the left-hand player the 4-pole switch S1 is closed. This produces several results. Firstly points X and Z are connected to ground via R38. This clears FF1 and presets FF2 so that when the ball is served it will travel upwards and to the right.
Point U (R51) is connected to positive supply, thus charging C32 rapidly and holding the ball off the left-hand side of the screen. Point T (cathode of D14) is connected to the emitter of T9, whose base is fed via R39 from P3 (left-hand bat control). The voltage on C31 is thus constrained to slightly above the emitter voltage of T9, thus determining the vertical position from which the ball will start. When the switch is released the constraints on C31 and C32 are released so the ball travels in a direction determined by the states of FF1 and FF2 (i.e. up and to the right).

Service by the right-hand player operates, so to speak the same way but backwards, i.e. pushing S2 grounds point X so that the ball still travels upwards. However, point Y is grounded so that the ball travels to the left, and point U is grounded to discharge C32 so that it starts from the right. The vertical starting position is determined by the emitter potential of T10.

Modulator and oscillator
The only part of the circuit which remains to be described is the modulator/oscillator which converts the video output at point A into a VHF signal suitable for feeding direct into a television aerial socket. This part of the circuit is shown inset in figure 3. An AF239 forms the basis of the oscillator circuit which is tuned to the required frequency by the coil L and C36/C37. The output may be fed direct into an unbalanced 50 - 75 Ω coaxial cable terminating in a normal TV coax plug, or if the TV has continental type 240 - 300 Ω twin feeder input then the output must be fed through an inverse balun transformer before feeding into the 300 Ω feeder.

Power Supply
A power supply which is absolutely free from mains ripple is absolutely essential for the TV Tennis game. The reason for this is fairly obvious. Any mains ripple will cause a variation in the input voltages to the trigger delay circuits, and hence in the trigger delays. This produces distortion of the picture as the trigger delay varies down the screen height. For portable operation a 6 V lantern battery or accumulator may be used, with a decoupling capacitor across the supply pins on the board (say 1000 μF), whilst for mains only operation the 5 V power supply shown in figure 4 is strongly recommended. It is based on an integrated circuit regulator the L129. This IC will provide a stabilised voltage of 5 V from inputs up to 20 V and will supply a maximum current of 600 mA. However, to minimise power dissipation within the IC it is recommended that a transformer with a 6.3 V RMS secondary voltage be used. This will give a D.C. input to the IC of about 9 V. The bridge rectifier is made up of 4 1-amp diodes such as 1N4001. Note that C3 should be a tantalum type to reduce output noise and any tendency to R.F. instability. Components D1, D2, R1 and R2 correspond with figure 3a.

Construction and adjustment
The p.c. board and component layout for the VHF oscillator are given in figure 5, for the main board in figures 6 and 7, and for the power supply in figure 8. A point-to-point wiring diagram is given in figure 9. Slider poten-
Figure 9. Point-to-point wiring diagram showing how the various boards are interconnected with each other and with the switches and potentiometers.
Tiometers are used for the bat controls as these give easier control than rotary types and are sufficiently robust for domestic use. The oscillator is mounted on a separate board as it must be housed in a completely screened box to avoid radiated interference and to minimise pickup of other transmissions. A small diecast or pressed aluminium box with a lid is suitable. The main board housing should also be a metal box. Having checked that the circuit is correct and that the power supply is giving the correct voltage before connecting it to the unit, power can then be applied and the output of the VHF oscillator plugged into a TV set. Due to the harmonics generated extending into the hundreds of MHz the unit will function on both VHF and UHF although the line oscillator frequency is of course different for 405 and 625 line reception.

Initially all the potentiometers should be set at the middle of their travel. If an oscilloscope is available the waveform point A can be checked, if not, then proceed as follows. For VHF operation the TV set should be tuned to channel 3 or 9, though with pushbutton tuning there is often no indication of to which channel the set is tuned to, so it must be tuned over the entire band until the signal is picked up. By adjusting the TV tuning and C36 it should be possible to tune in the signal. At first the picture will be rather chaotic as the field and line sync oscillators are not running at the correct frequency. By adjusting P1 it should be possible to obtain vertical lock, i.e. the picture will stop 'rolling'. Of course with mains field sync there is no adjustment and if lock is not obtained it will be necessary to adjust the frame hold control on the TV set.

It may be found that, due to the tolerances of C1 and C2 it is not possible to obtain the correct field sync frequency. The oscillator may run at 25 Hz, in which case the picture will lock but will jitter considerably. In this case C1 and C2 should be reduced to 2 µF. It may be found that a black bar appears in the centre of the screen. This is because the field sync oscillator is running at 100 Hz, and P1 should be adjusted until normal lock is obtained.

Having obtained vertical lock the picture will probably consist of a random pattern of white dashes. P2 can now be adjusted until the two black bats appear on the screen. If the line sync oscillator is tuned to a multiple of the line frequency then four bats may appear. Having obtained the correct number of bats the horizontal positions of the left- and right-hand bats may be adjusted by P4 and P5 respectively.

The final adjustment is to the range of the vertical bat controls. With the slider controls set to the centre of their travel P5 and P8 are adjusted so that the bats are halfway down the screen. It should now be possible to traverse the bats over the entire screen height, and some further slight readjustment of P5 and P8 may be necessary to achieve this.

The unit is now ready for use and should be possible to serve a ball from either side of the screen by pressing the appropriate service button. Due to the simple nature of the circuit it may be found that pressing the service button causes slight picture jitter, but this should not prove inconvenient in practice.

---

### Parts list for figures 4 and 8

**Resistors:**
- R1, R2 = 470Ω

**Capacitors:**
- C1 = 470µF/16V
- C2, C4 = 100n
- C3 = 10µF/6V (tantalum)

**Semiconductors:**
- D1 = DUS
- D2 = 4.7V zener
- B = Bridge rectifier, or 4 x 1N4001
- IC1 = L129

**Sundries:**
- Transformer, 6.3...8 V (r.m.s.) secondary
frequency counter

Logic IC’s are nowadays so cheap that it is possible to build a digital frequency counter for a very small outlay. The circuit described here is based on the popular 74 TTL logic family. The first part deals with the basic counter, and in a subsequent article additions to the instrument will be described.

**Specification**

- **Input sensitivity (frequency measurement)**: 1.7 V p-p.
- **Input sensitivity (period measurement)**: 2.6 V p-p.
- **With an input risetime of 0.5 μs/V.**
- **Maximum input frequency**: 18 MHz.

In its basic form the instrument is a six-digit frequency/period meter. The basic counter/latch/display is shown in figure 1, which is the circuit of two stages of the counter, showing how the 7490’s are cascaded, and how the interconnections between the latch and reset inputs are made. The segment series resistors are shown dotted, as the circuit may be used with either Minitron or LED displays, and series resistors are not required with Minitrons.

A p.c. board for one stage of the counter/latch/display decoding is given in figure 2. Six of these boards are required for the six-digit counter. The displays are all mounted on a single board to which the counter boards are wired, either with wire links, as in figure 3, or if LED displays are used, via segment resistors, as in figure 4.

Figure 5 shows the pinout and voltage/current curve for a Minitron display type 3015F. Note that for use with a 447 decoder the points shown as round are in fact commoned to +5 V.

A p.c. board for use with Minitron displays is shown in figure 6, and the component layout in figure 7, showing the connections to a counter board.

---

**Parts list for figure 1**

**IC’s:**
- IC1 = 7490
- IC2 = 7475
- IC3 = 7447

**Resistors:**
- $R_1 = 1 \text{k }$
- $R_b \ldots R_g = 180 \text{ }$ (LED display only)

---

**Figure 1. Two stages of the counter/latch/display circuit, showing how the counters are cascaded.**
Figure 2. P.c. board for one decade of the counter, latch and display driver.

Figure 3. Component layout for figure 2 using Minitron displays.

Figure 4. Component layout for figure 2 showing segment resistors for LED displays.

Figure 5. Pinout and characteristics of Minitron.

Figure 6. P.c. board for Minitron display.

Figure 7. Component layout for Minitron display.

Figure 8. Pinouts of three popular LED displays.

Figure 9 shows the corresponding board for use with LED displays. Most common anode LED displays are pin compatible with respect to the cathode (segment) connections, but some types have multiple anode connections (usually pins 3 and 9). These are catered for on the board, but if a display is used that does not have anode connections to these pins it may or may not be necessary to cut them off, depending on whether or not they are N.C. (no connection).

The pin connections of three popular LED displays are given in figure 8. For further data on common-anode LED displays see Elektor No. 3 page 451.

Photographs 1 and 2 show the general appearance of the display/counter board assembly, and also how the segment resistors are soldered to the back of the display board when using LED displays.

Control logic

To make the decade counter just described function as a frequency counter various control signals must be applied to it. Firstly, the pulses to be counted must be gated into the first stage of the counter. Secondly, after the counting period has ended the count must be stored in the latch. The counter must then be reset ready for the next count. All these functions are performed by the control logic, the circuit of which is given in figure 10.

The counter will operate in two basic modes, frequency and period. In the frequency mode incoming pulses are counted for a period of time depending upon the counter gate period. Thus if the incoming frequency was 100 kH and the gate period 1 s then the count displayed would be 100000.

In the period mode the internal frequency reference of the counter is itself counted and is gated by one cycle of the incoming signal. Thus, if the internal reference frequency was 100 Hz, and the signal to be measured had a period of 1 s, then the count displayed would be 000100. Of course the decimal point on the display board can be shifted so that this could be displayed as 1.00 (see below).

The control logic operates as follows. In
the basic version of the frequency counter the reference frequency is derived from the 50 Hz mains. This is adequate for many applications, but provision is made for the addition of a crystal-controlled reference for greater accuracy and versatility.

The 50 Hz reference is taken from the secondary of the mains transformer that supplies power to the counter. The A.C. waveform is rectified by the bridge thus providing a 100 Hz full-wave rectified waveform. This is fed to the input of S1 (7413 NAND Schmitt trigger) via R1, and is clamped to 4.7 V by D1. The 100 Hz pulses from the output of S1 are divided down to 50 Hz, 10 Hz, 5 Hz, 1 Hz and 0.5 Hz by FF1, IC4 and IC5. The 50 Hz, 5 Hz and 0.5 Hz outputs are used to provide 10 ms, 100 ms or 1 s gate periods depending on the position of switch S1.

For ease of operation, a fifth deck of S1 can be used to switch the decimal point (figure 10b). The switch positions can then be labelled 'MHz', 'kHz' and 'sec'.

In the first three positions of S1 the gate pulse is fed from S1b into Schmitt trigger S2, together with the signal to be measured. Thus when the gate signal from S1b is a logic '1' the signal to be measured is allowed through S2 to the counter input. The latching and reset signals are derived in the following manner, referring to the timing diagram figure 11.

During the gate period (waveform B from S1b 'high') the gating signal E holds pin 9 of N1 and pin 11 of N2 high. The outputs C (to latch) and D (to reset inputs of counter) are thus low. The latch is thus in the 'store' mode and the reset inputs of the counter are low, so the counter counts the pulses which are gated through S2 to output E by the gating signal.

At the end of the gate period waveform B and waveform A (from S1a) both go low. A is connected directly to pin 8 of N1 and B is connected via R4 and C1. The negative-going edge of B is differentiated (B'). N1 performs the logic function \( C = A + B \) so a short positive-going pulse appears at output C, momentarily putting the latches into
the 'enable data entry' mode and thus storing the count. This pulse also triggers the monostable IC6, which performs several functions. Firstly, its Q output holds the input to S1 high, thus blocking the 100 Hz pulses to FF1. It also holds pin 12 of N2 high, so the output remains low. The Q output clears FF1. When the monostable resets the timebase will restart. The next positive transition of the A signal will be inverted by N3, and the input (pin 12) of N2 will be pulled low by R5. Since the other input is connected to the B signal, which is already low, the output of N2 goes high for the duration of the positive A pulse, thus resetting the counter. When the B signal goes high again the counter commences another count and the sequence repeats. D4 lights when the gate is open.

The pulse length of the monostable IC6 can be varied by P1. It is apparent that this pulse length determines the time for which the timebase is disabled, and hence the interval between counts. This facility is useful, as with a short count interval the continual variation in the last digit can be annoying. A longer count interval will alleviate this. On the other hand, when a rapid succession of measurements is to be taken then a short count interval is useful.

**Period Measurement**

To measure the period of the incoming...
waveform the 100 Hz reference is counted whilst the gate, latch and reset functions are derived from the signal to be measured. To do this the switch S1 is set in position 4. This disables the time base, connects the gate input of S2 to the Q output of FF2 and connects the 100 Hz signal to the other input. It also connects the latch circuitry input A to the incoming signal. The sequence of operations is thus as follows: on the first negative transition of the input signal H FF2 clocks and its Q output goes to '1' thus opening the counter gate. 100 Hz pulses (G) are now gated through S1 (E) and are counted. On the next negative transition of the input signal the flip-flop FF2 again clocks and the Q output goes to '0', thus closing the gate. The gate period is thus one complete cycle of the input waveform. The input waveform drives the latch reset circuitry in a similar manner to
that for a frequency measurement, and the timing diagram is shown in figure 12. Of course, the A signal is now the input signal, and the B signal is the Q output of FF2.

With a 100 Hz reference frequency and
Parts list for figure 15

Resistors:
- \( R_1, R_2 = 3k\Omega \)
- \( R_3 = 6k\Omega \)
- \( R_4 = 470 \, \Omega \)
- \( R_5 = 100 \, \Omega \)
- \( R_6 = 180 \, \Omega \)
- \( R_7 = 1 \, k\Omega \)
- \( R_8, R_9, R_{10} = 1 \, \Omega \)
- \( P_1 = 1 \, k\Omega, \) preset

Capacitors:
- \( C_1, C_2 = 100 \, nF \)
- \( C_3, C_4 = 1 \, nF \)
- \( C_5 = 2200 \, \mu F, 16 \, V \)
- \( C_6 = 220 \, \mu F, 4 \, V \)
- \( C_7 = 10 \, \mu F, 16 \, V \)
- \( C_8 = 470 \, \mu F, 6.3 \, V \)

Semiconductors:
- \( B_1 = \) bridge rectifier B20 C2200
- \( D_1 = 3 \, A \) diode
- \( D_2, D_3 = \) DUS
- \( D_4 = \) zener 4.7 V, 400 mW
- \( T_1 = T_{UP} \)
- \( T_2, T_3, T_5 = T_{UN} \)
- \( T_4 = T_{IP} \, 2955 \)

Sundries:
- \( F_1 = \) fuse 2.5 A slow blow
- \( T_{r1} = \) transformer 12 V, 2 A
figure 15. Power supply for frequency counter.

figure 16. P.c. board and component layout of power supply.

The gate periods of 10 ms, 100 ms and the period of the instrument is limited. It is only possible to obtain a full-scale reading in the period mode when the period is 9999.99 seconds. For a period of 1 s the display will be only 000100, a resolution of one part in a thousand. Clearly, for short period measurements a higher reference frequency is necessary to obtain a larger count and hence a better resolution. Provision is made for feeding in an external reference frequency by breaking the circuit at the point marked 'EXT LEF'. In the frequency mode the maximum and minimum frequencies which can be measured are limited by the gate periods. For instance with a 1 s gate period a frequency of 100 Hz will only be measured with a resolution of one part in a hundred, whilst with a 10 ms gate period an input frequency of greater than 99.9999 MHz would cause the counter to overrange. However, since the upper frequency limit of the TL counters used in the circuit is only 8 MHz anyway, this problem does not arise.

A printed circuit board and component layout for the control logic board are given in figures 13 and 14, showing the connections to the switch.

Power supply

A suitable power supply for the frequency counter is shown in figure 15. This is well decoupled against mains-borne interference and has a 100 Hz output for the reference frequency. A board and component layout for the power supply are given in figure 16. As the complete frequency counter draws about 2 amps, the series regulator transistor T4 should be mounted on an adequate heatsink. If the unit is housed in an aluminium case then the back of the case should prove suitable.

In future issue we shall be describing additions to the frequency counter, notably an input preamplifier to increase the input sensitivity.

J.P. Kuhler jr.

humming kettle

Those who have in the course of time lost the whistle of their domestic kettle and the unfortunate ones who do not possess a whistling kettle at all, who must boil water without the aid of an acoustic signal, are encouraged by the author not to resign themselves to this unsatisfactory situation. A very modest amount spent on components together with a little work puts a 'humming kettle' within everyone's grasp!

The circuit is so simple that further explanation is hardly necessary. As the temperature increases, the resistance of the NTC drops until at a certain moment (adjustable with P1) transistor T1 cuts off, so that T2 conducts and the buzzer is activated.

R. Buggle

active flash slave

For those who have often been annoyed by badly illuminated flash photographs and also dislike the tangle of cables involved in using two flashguns, the flash slave is the only solution. The author spent quite some time building several slave units before arriving at the design presented here, which has the advantages that it requires no separate supply voltage and that both electronic and ordinary flashguns can be operated

Four silicon photovoltaic cells (BPY 11) form a light sensor. Undoubtedly other types will do, too. The thyristor must be of a type with a very low firing voltage; the TIC 46 used here performs quite well. The circuit itself needs little comment: only that the polarity of the flash connection should be correct; the 'plus' should be connected to the centre pin of the connecting cable. The circuit can best be housed in a small, transparent plastic box.

Of course the circuit must be mounted in, on, or in the immediate vicinity of the kettle.
NAND gates N1, N2 and N3, N4 (IC4 = CD4001) make up two touch switches. Four LEDs are used to indicate the condition in which the system has been set; D2 = ON, D3 = OFF, D6 = headphones and D5 = power amplifier.

Because of the difference between this circuitry and the rest of the TAP system, construction is much simpler: instead of a diode matrix only two flip-flops are used here.

The power supply is split up into three sections: one for the touch switches, one for the rest of the TAP preamp and one for the disc preamplifier.

The supply for the touch switches must stay in operation even in the 'OFF' condition, because it would not otherwise be possible to start the whole outfit with the 'ON' touch switch. For this reason, the switch supply is drawn directly from the unstabilised supply via series resistor R15 and zener diode D1.

Integrated voltage stabiliser IC3 stabilises the 10-V supply needed for the TAP pre-amp. This can be accurately adjusted with preset potentiometer P1.

As the maximum output current of this IC is only 150 mA, the external power transistor T1 is added. When the supply voltage is switched on with the 'ON' touch switch, the logic state prevailing at the output of gate N1 is '1', while it is '0' at the output of N2. Transistors T2 and T3 are therefore cut off, and the supply voltage becomes available at output C.

When the 'OFF' panel is touched, logic levels at the outputs of N1 and N2 are reversed, with the result that T2 and T3 turn on. The potential at pin 13 of IC3 is therefore pulled down almost to zero, so that the internal output transistors in the IC are cut off. The voltage at output C drops to 0 and the TAP preamp is turned off.

The flip-flop formed by N3 and N4 provides a changeover between headphones and the main power amplifier. When the output of N3 is at logic '1', transistors T5 and T6 turn on, switching on the headphone amplifier built around T7 and T8. This amplifier, including the associated components within the dashed rectangle in figure 1, is duplicated on the board for the left-hand headphone channel. Both amplifiers derive their supply from the collector of T6. The output of N4 is at logic '0'. Transistor T4 is cut off and relay Re is not energised. The relay contacts,
which switch the supply for the main power amplifiers on and off at the primary of the mains transformer for these amplifiers, stay open. When the loudspeaker touch panel is touched the relay contacts close and the power amplifier is turned on: the headphone amplifier no longer gets a power supply because the logic '0' at the output of gate N3 cuts off transistors T5 and T6.

The disc preamplifier (figure 2) is the same as was described in the April 1975 issue of Elektor. Power supply for the preamplifier is provided by the integrated stabiliser IC2. Points A and B are connected to the corresponding points in figure 1.

**Construction**

Current consumption of the touch-switching circuit is about 30 mA in the 'OFF' position. In the switched-on state, the maximum consumption with headphone listening is about 100 mA (not counting the TAP preamplifier, of course!). Including the TAP preamplifier, the maximum current consumption is 320 mA when the headphone amplifiers are on and the volume control is at maximum.

Figure 1 shows six points at which the D.C. voltage can be checked. With the transformer secondary delivering 16 volts RMS and the TAP preamp not connected, the voltages at these points should be 20 V, 10 V, 12 V, 6.8 V, 1.8 V and 6 V respectively.

The headphone amplifier delivers 2 V R.M.S. with the maximum input signal of 850 mV. Headphones with an impedance of 400 ohms or higher can be

---

**Parts list for figure 1**

**Capacitors:**
- C18 = 2200 μF/35 V
- C19, C23 = 220 μF/16 V
- C20 = 330 nF
- C21 = 470 nF
- C22 = 4 μF/16 V
- C24 = 100 μF/25 V

**Resistors:**
- R15, R35 = 680 Ω
- R16 = 0.68 Ω
- R17 = 1 kΩ
- R18 = 3 kΩ
- R19, R28, R31, R36 = 470 Ω
- R20, R21, R22, R23 = 10 MΩ
- R24, R26, R27, R29, R32 = 27 kΩ
- R25 = 220 Ω
- R30 = 10 kΩ
- R33 = 6 kΩ
- R34 = 1 k5
- R1 = 1 kΩ

**Sundries:**
- Transformer = 240 V/16 V, 1 A (see text)
- Bridge rectifier = BA40C1500
- Relay R0 = 10 V, 300 Ω (see text)

**Semiconductors:**
- D1 = 5V6/400 mW
- D2, D3, D5, D6 = LED
- D4 = DUS
- T1 = BD 135 (cooled)
- T2, T6 = BC 177 (possib. TUP)
- T3, T5, T8 = BC 107 (possib. TUN)
- T4 = BC 517
- T7 = BC 549 C, BC 109 C
- IC3 = μA 723
- IC4 = CD 4011
Figure 2. Circuit of the disc preamplifiers, and external connections to the TBA 625C stabiliser IC from which they are supplied.

Figure 3. Printed circuit board and component layout.

Parts list for figure 2

Capacitors:
- C1, C15 = 680 p
- C2, C6, C10, C14 = 4 µF/25 V
- C3, C13 = 2 n
- C4, C5, C11, C12 = 4 n
- C7, C9 = 470 n
- C8 = 10 µ/16 V
- C16 = 100 n
- C17 = 10... 22 µ/25 V

Resistors:
- R1, R14 = 100 k
- R2, R13 = 1 M
- R3, R11 = 10 Ω
- R4, R12 = 1 k
- R5, R10 = 270 k
- R6, R9 = 150 k
- R7 = 56 k
- R8 = 470 k

Semiconductors:
- IC1 = SN 76131, µA 739, TBA 231
- IC2 = TBA 625 C
It is often a good solution to use the case as a heat sink, with the transistor mounted on the outside.

The pull-in voltage for relay Re is about 10 V. The contacts must be rated to make and break at least 250 V, and a current depending on the maximum drawn by the power amplifiers. For two 100 W amplifiers driving 4-ohm loads a relay with 8 A contacts is suitable.

To avoid relay chatter when a number of touch panels are operated at the same time, it is advisable to connect 1 n capacitors $C_a$ to $C_d$ across each pair of touch contacts.

A 100 n/400 V capacitor can be connected across the relay to prevent contact burning.

The TBA 625C stabiliser IC delivers an output of 15 V. As this is the minimum acceptable voltage for the disc preamplifier, it is essential that a Type C stabiliser be used. A heat sink is not absolutely necessary. A tantalum electrolytic capacitor should be used for $C_{17}$ to forestall any possible tendency to oscillation.

Figure 3 shows the printed circuit board and the component layout for the TAP-power circuit. Except for the mains transformer, bridge rectifier, smoothing capacitor $C_{18}$ and relay, all the components are accommodated on one board.

### Transformer secondary voltage

<table>
<thead>
<tr>
<th>Transformer secondary voltage (V RMS)</th>
<th>Heatsink area (cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>50</td>
</tr>
<tr>
<td>18</td>
<td>80</td>
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</table>
Any horologist who keeps a digital clock in the same room as conventional clocks cannot but feel sad to see it sitting there, mute and reproachful amongst its more vociferous brothers, its only sound the feeble humming of the mains transformer. In this article we look at various ways of providing the digital clock with a voice, so that it can draw our attention to the fact that it is keeping time far more accurately than any mere mechanical clock.

The main attribute lacking in a digital clock is the comforting tick which assures us that the thing is actually going. How many man-hours have been wasted waiting for the elusive change of that last digit? ‘Well I’m sure it’s been stuck at that time for more than a minute now.’

A clock with a seconds display or flashing colon alleviates these problems, but the hypnotic effect of such devices has been known to send people to sleep. No such problem exists with a tick, which informs us that the clock is working without actually looking at it.

The circuit
The tick-tock sound of a conventional clock is produced by the balance wheel (or pendulum) and escapement, the tick and tock sounds having different pitch. The pitch of the sounds and the repetition frequency obviously depend on the physical construction of the clock. A grandfather clock will have a deeper, more leisurely tick than a travelling alarm.

Electronic simulation of the sound is fortunately relatively simple. The waveform of the ticking is a damped res-
onence similar to a percussion instrument. A suitable circuit is therefore the gyrator used in the Elektor Minidrum (February 1975). This circuit (with the component values modified for this application) is given in Figure 1. Suitable 1 Hz trigger pulses may be obtained from the clock circuit by taking an output from the counter preceding the seconds counter. The pulses must be TTL compatible (5 V amplitude) and have a 1:1 mark-space ratio, otherwise the ticking will sound unbalanced. The pulses are fed into the base of T3 through C3 to trigger the gyrator, whilst T5 switches C2 in and out of circuit to alter the relative frequency of the tick and tock.

Components list for figure 1

Resistors:
R1 ... R9, R11 = 6k8
R10 = 1k5

Capacitors:
C1 = 4n7
C2 = 1n8
C3 = 1 n
C4 = 6n8
C5 = 100 μ/10 V
C6 = 100 n

Semiconductors:
T1, T3, T5, T6 = TUN
T2, T4 = TUP
D1, D2 = DUS

This article is based in part on suggestions made by:
H. F. Daems (alarm) and
J. P. Vos (Time signal).
The frequency of the sounds may be adjusted to suit personal taste by experimenting with the values of C1, C2 and C4. Since C3 and the input impedance of the trigger input differentiate the trigger pulse, changing the value of C3 will affect the 'crispness' of the sound.

P.C. Board
A suitable printed circuit board already exists for the Minidrum gyrator, and the board and component layout (modified for use with clock) are given in figure 2.

Alarm Clock
One clock noise in popular demand by readers (though perhaps not first thing in the morning) is an alarm. It is a simple matter to add an alarm to a digital clock (but unfortunately not so simple if the display is multiplexed). The alarm control circuit given in figure 4 is suitable for TTL clocks with parallel outputs (i.e. where the BCD outputs of the hours and minutes counters are available continuously and are not strobed). It was felt that an alarm setting accuracy of one minute was not necessary, so the smallest step provided in this circuit is 10 minutes.

The circuit operates as follows:
the portion of the circuit inside the dotted box is the alarm. The rest is the existing clock circuitry. The BCD outputs of the hours and tens of minutes counters are decoded to decimal by the 7442's. No decoding of the tens of hours is required as the truth table for this counter (table 1) shows. Outputs A and B are never both '1' at the same time. The desired alarm time is selected by single-pole switches S1 - S3. When the required time is reached three of the inputs of the four-input NAND gate go high. This allows the alarm signal connected to the fourth input to pass through the gate.

The possibilities for the actual alarm signal generator are endless. The simplest solution would be a fixed frequency oscillator such as an astable multivibrator. There are however more interesting possibilities. The voltage-controlled multivibrator of figure 5 can be made to play a tune by connecting differing voltages sequentially to the control input. For a control voltage range of 2-5 V the frequency range covered is about 3 octaves. There are various methods of driving the oscillator. A simple circuit is shown in figure 6. This consists of a 7490 connected as a BCD decade counter, with its outputs connected to the VCO via presets. As the

| Table 1 |
|---------|-----|-----|-----|
| HOURS | A   | B   | B   |
| 0     | 0   | 1   | 0   |
| 10    | 1   | 0   | 0   |
| 20    | 0   | 1   | 1   |
output states of the counter change so will the output voltage to the VCO. Of course the outputs change in a binary sequence so more than one output can be high at one time. Since the outputs interact it is difficult to set this circuit to play a particular tune. In addition the 1 Hz clock pulses are also fed in via R2 increasing the permutations still further. If one requires a circuit which can be set to play a particular tune then figure 7 is more suitable. Here the outputs of the 7490 are decoded with a 7442 to give ten independent outputs. These outputs go low in sequence as the counter goes through its cycle. All other outputs are high, reverse-biasing their respective diodes, so no current flows through their respective presets. Only the preset connected to the output which is low forms a potential divider with R1. This means that each note in the sequence can be tuned independently.

This ten-note sequence can easily be extended to twenty notes by the circuit of figure 8. In this circuit two decoders are driven by the 7490 and are switched in and out by the 1 Hz clock pulses to the counter. Thus, during the half-period when the clock pulse is '0' the outputs of the 7490 are switched through the transfer gates (7400) to decoder A. The other transfer gates are disabled by the '0' on their commoned inputs, so their outputs are all '1'. This is an invalid input code for the 7442 so all its outputs are high. During the '1' half period of the clock pulse the reverse situation occurs. Decoder B is enabled, whilst A is disabled. Decoder A thus controls the even notes 0, 2, 4, ... in the sequence, whilst decoder B controls the odd notes 1, 3, 5, ... Of course in this case, if an equal time span is required for each note then the clock pulse waveform must have a 1 : 1 mark-space ratio. The 7490 in all these cases can be the existing seconds counter in the clock. Another variation on the alarm theme can be obtained by a circuit which changes the rhythm of the tone sequence, making it less monotonous. Such a circuit is given in figure 9. The dividers I to III are again part of the existing clock circuit. The operation of the circuit is as follows:

counter II controls the pitch of the voltage controlled multivibrator as in the circuit of figure 6, except that no adjustment is provided for. The time at which the alarm sounds is again determined by the alarm control circuit, as in figure 4. The rhythm variation is provided by gating the C output of counter I with the A output of counter...
III, and the B output of counter I with the B output of counter III. This has the following effects. Starting at a point in the timing cycle where counter III has just reset A4 and B4 are both '0'. The outputs of N1 and N2 are thus high so (assuming it is time for the alarm to go off and the outputs of N3 and N4 are high) the tone sequence controlled by counter III can pass through N5. After 10 seconds output A4 goes high and the pulses from output C2 switch the output of N2 between '0' and '1'. The tone from the output of N5 is thus switched on and off at a 2.5 Hz rate. After 20 seconds output B4 goes to '1' whilst output A4 goes to '0'. The output of N2 is thus high whilst via N1 output B3 switches the tone on and off at a 5 Hz rate. After 30 seconds output B4 again goes to '1' while A4 remains at '1'. Outputs B2 and C2 therefore both affect the tone output. When either of these outputs is high the tone is off, and when both of them are low the tone is on.

A timing diagram for these events is shown in figure 10. The top two waveforms are the outputs B2 and C2 during a 1 second interval of the sequence (this repeats every second). The other 4 waveforms are the tone outputs that occur for the four possible states of A4 and B4.

The audible effect is thus as follows: an uninterrupted tone sequence for 10 seconds, then a further 10 second interval of tone bursts and silence as in figure 10d, then 10 seconds as figure 10e and finally 10 seconds as in figure 10f, after which the sequence repeats.

Of course, during each ten second period the frequency of the tone is being varied by the outputs of counter II. It should be noted that for all these alarm circuits a symmetrical 1 Hz squarewave is required from the output of counter II. This means that the 7490 (which consists of a divide-by-2 and a divide-by-five counter in the same package) must be connected with the divide-by-2 after the divide-by-5, as shown in figure 9. If an existing clock circuit is used this counter may be connected as a BCD decade counter (i.e. with the divide-by-5 after the divide-by-2). Some slight modification may therefore be necessary.

**Volume Control**

In order not to awaken the sleeper too harshly it is a simple matter to arrange a volume control so that the alarm tone starts at a low level and gradually becomes louder and louder until it is switched off. This is achieved by the circuit of figure 11. The counter shown is the minutes counter (i.e. the one that drives the minutes display). Since the alarm can only be set in units of ten minutes, the alarm will sound when the tens of minutes have just changed to the required number and the minutes counter is reset. Outputs A to C of the minutes counter are thus at '0', so T2 to T4 are turned off. The alarm tone is applied to the base of T1 via R1 and switches this transistor on and off, causing a signal from the loudspeaker.

Since there is a 390 Ω resistor (R2) in series with it the tone is not very loud. After 1 minute the A output of the counter goes to '1', switching on T2 and thus connecting R3 in parallel with R2. The tone thus becomes louder. After 2 minutes output B becomes '1' while A becomes '0'. R4, which is smaller than R3, is paralleled with R2, so the tone becomes louder still. After 3 minutes outputs A and B are '1', and after 4 minutes output C becomes '1', by which time the tone is quite loud.

Output D is not connected to this system. If the sleeper has not awoken after 8 minutes output D will become '1' and can be connected to set off a small explosive charge underneath the bed. A less drastic cure for the deep sleeper is to connect an additional transistor to output D with a 56 k ohm resistor in series with its emitter.

The complete circuit of an alarm system is given in figure 12. Everything within the dotted box is the alarm circuit, whilst everything outside is the existing clock circuit. This differs slightly from the circuits discussed in that a HEX-inverter replaces the five-input NAND-gate in the alarm control circuit. This has open-collector outputs, so the outputs may be joined to perform a wired-OR function. In this circuit the additional transistor T9 is shown connected to output D5 for the extra loud alarm signal. A suitable printed circuit board and component layout for this alarm are given in figure 13.

**Time Signal Generator**

Provision of a 'six pips' time signal every hour is a relatively simple matter.
Components list for figure 12

Resistors:
- R1 = 39 k
- R2 ... R5 = 47 k
- R6 = 18 k
- R7, R12, R13 = 1 k
- R8, R11 = 12 k
- R9, R10 = 1 M
- R14, R18 = 390 Ω
- R15 = 180 Ω
- R16 = 120 Ω
- R17 = 56 Ω

Capacitors:
- C1, C2 = 1 nF

Semiconductors:
- T1 ... T9 = TUN
- D1, D2 = DUS

IC's:
- IC1 = 7401
- IC2, IC3 = 7442

Switches:
- S1 = single pole 6-way
- S2 = single pole 10-way
- S3 = single pole 3-way (decimal coded thumbwheel switches suggested)
and a suitable circuit is given in figures 14 (block diagram) and 15. The portion of the circuit outside the dotted box in figure 15 is the existing seconds counter in the clock. The circuit works in the following manner: the inputs of gate 1 are connected to the outputs of the tens of minutes, minutes, tens of seconds and seconds counters corresponding to the time 59 minutes 55 seconds. When this time is reached the inputs of gate 1 will all be high, so the output will be low. At any other time at least one input must be low, so the output will be high. Normally therefore, the Q output of IC2 is low, so the output of IC4b is high blocking the oscillator IC4a (which will be dealt with later), whilst the Q output is high, holding the +6 counter IC3 in

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Figure 13. P.C. board and component layout for the circuit of figure 12.

Figure 14. Block diagram of a time-signal generator.

Figure 15. Complete circuit of the time-signal generator.
the reset condition. On the negative-going edge of the incoming seconds pulse at 59 minutes 55 seconds the output of the seconds counter will assume the condition '5', i.e. outputs A and C high. The output of gate 1 will go low, clearing IC2 so that the Q output goes low and the Q output goes high.

IC3 may now count the incoming seconds pulses. However, due to the propagation delays through the seconds counter, IC1 and IC2, it will not count on the abovementioned negative-going edge, as this has already disappeared before the counter is enabled. However, the negative-going pulse is differentiated by C1 and R3 (neglecting R1 and the base resistance of T1), and turns off T1 for about 100 ms. This takes pin 1 of IC4 high, and since pins 4 and 5 are already held high by the Q output of IC2 the oscillator will be gated through it providing a 1 kHz tone burst of 100 ms duration.

On each negative-going edge of the five subsequent second pulses IC3 will count and the oscillator will provide a 100 ms tone burst. On the fifth pulse the D output of IC3 will go high, and on the sixth pulse the D output goes low, clocking IC2, so that its Q output goes high and its Q output goes low. This disables the oscillator and holds the counter (IC3) in a reset condition so that it can count no further seconds pulses. This condition obtains for a further 59 minutes 55 seconds until it is time for the next signal.

The circuit thus produces six pips every hour, starting with the first pip at 59 minutes 55 seconds and terminating with a pip exactly on the hour. Of course, this circuit produces pips of equal length, whereas the last pip of a radio time signal is longer than the preceding five. An alternative circuit, which produces this type of signal, was described in Elektor July/August 1975.

Oscillator and Amplifier

The oscillator is a simple single time
constant multivibrator based on the 7413 which is a dual 4-input NAND Schmitt Trigger. Assuming the output of IC4a is initially high then C2 will charge through P1 until the voltage across it reaches the threshold of the Schmitt trigger. The output will then go low and C2 will discharge through P1 until it falls below the threshold, when the output will go high again. Because of hysteresis the negative-going threshold is below the positive-going threshold, so the frequency of the oscillator is determined by the time taken to charge and discharge C2 between these points, which is of course dependent on the time constant P1C2. The oscillator frequency can therefore be varied by P1. With $C_2 = 1 \mu F$ and P1 set to 330 $\Omega$ the frequency will be about 1 kHz. Altering P1 also changes the mark-space ratio of the waveform, but this is unimportant in this application.

The other gate in IC4 is used to gate the oscillator output into the amplifier, consisting of T2 to T3. This is a simple switching amplifier, as only square waves are being dealt with. In the quiescent state only T2 is turned on so the current drawn is only about 7 mA.

P.C. Board

The track pattern and component layout out of a board suitable for the time-signal circuit is given in figure 16. Note that R4 (shown dotted in figure 15) is a precaution against power supply ripple appearing at the loudspeaker output. Depending on the power supply it may or may not be necessary.

Figure 16. Board and component layout for the time-signal generator.
lie detector

This lie detector works in the usual manner by measuring skin resistance and therefore is no innovation, but in comparison with the designs popular some years ago it offers a number of useful improvements. In the circuit the advantages of opamps have been turned to full use. The detector operates fully symmetrically, and therefore two batteries are required. The voltage across the electrodes according to local regulations in some countries, may not be higher than 2 V so a reference voltage of no more than 1.2 V is applied to the input of the measuring bridge. Since the resistance of the human skin is generally 50 k or less, the voltage across the electrodes will be at maximum 0.6 V. The set-up of the measuring bridge has the additional advantage that the reference voltage is independent of the battery voltage. To obtain a sufficiently high sensitivity the total amplification in the detector should preferably be greater than 100,000 times. Therefore a second opamp was added, which brings the overall amplification to about 250,000 times. With the double potentiometer of 500 k the amplification can be adjusted from 0 to the above-mentioned maximum. The 100 k potentiometer serves to adjust the sensitivity of the moving coil meter; therefore the input bridge is first brought completely out of balance to the one side and then to the other by means of the 100 k potentiometer, whilst the positive and negative deflection of the meter is adjusted to maximum. Afterwards the adjustment potentiometer can, if required, be replaced by a fixed resistor.

brake lights for model cars

This circuit performs two functions: when the supply voltage to the motor of the model car cuts out, the car will not stop abruptly but will continue over some distance and during that time two LED’s will light up and function as brake lights. Thus a very realistic effect is obtained. The circuit is extremely simple. As long as the car is under power, there is a voltage across the motor (M), the polarity of which is indicated in the diagram. Capacitor C_1 and (via diode D) also C_2 are now charged. When the voltage cuts out, C_1 discharges across M and C_2 discharges via the two LED’s, resistor R, and motor M. If braking is the result of a short-circuit of the supply voltage, both capacitors discharge via the short-circuit connection; in that case the LED’s burn somewhat brighter. The value of resistor R can be calculated with the following simple formula:

\[ R = \frac{12 - 2 \cdot V_{LED}}{I_{LED}} \]

Usually a value of about 560 \( \Omega \) will be suitable.
Most of the integrated PLLs now available for FM receivers are expensive and require a 24-volt power supply, which makes them inconvenient for either portable or car-borne use. This universal PLL works quite happily on a 5-volt supply, but the working voltage may be determined in practice by the needs of a MOSFET RF amplifier, which can require 9 volts. This, however, is easy to provide in battery-powered portable equipment, and it also leaves a margin for stabilisation when running from a 12 V car supply.

Sensitivity on a 10.7 MHz FM input with 3 kHz deviation is 3.2 µV for a 700 mV audio output.

For a receiver for the 144 to 146 MHz band, the aerial signal is pre-amplified and converted to a band from 10 MHz to 12 MHz by a stable 134 MHz mixer-oscillator. Any signal in the 2 MHz-wide band can then be tuned in by adjusting (with a potmeter) the frequency of the voltage-controlled oscillator incorporated in the PLL.

Figure 1 shows a block diagram of the arrangement. The 134 MHz local oscillator will normally be a crystal oscillator of lower frequency in conjunction with a multiplier. Assuming the combined gain of the pre-amplifier and the mixing stage to have the easily-achievable value...

---

**Performance Data**

| Narrow-band FM reception (VCO free-running frequency approximately 10.7 MHz) |
|-----------------------------------------------|------------------|------------------|
| Capture and hold ranges                      | Capture | Hold |
| Input 160 µV                                 | 190 kHz | 540 kHz |
| Input 1.6 mV                                 | 250 kHz | 4 MHz  |
| Input 10 mV                                  | 400 kHz | 10 MHz |

<table>
<thead>
<tr>
<th>AM Suppression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input 160 µV</td>
</tr>
<tr>
<td>Input 100 µV</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Sensitivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deviation = ±3 kHz</td>
</tr>
<tr>
<td>Minimum input = 3.2 µV</td>
</tr>
<tr>
<td>With input = 4 µV: output = 700 mV, signal/noise ratio = 40 dB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Wide-band Stereo FM reception (VCO free-running frequency approximately 455 kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capture and hold ranges</td>
</tr>
<tr>
<td>With minimum input (12.6 µV):</td>
</tr>
<tr>
<td>Capture range = hold range = 400 kHz</td>
</tr>
</tbody>
</table>

| Sensitivity (Deviation = ±30 kHz)                                           |
| Minimum input = 12.6 µV                                                     |
| With input = 500 µV: output = 360 mV, signal/noise ratio ≥ 40 dB |

---

Elektor has taken a lead in drawing attention to the possibilities of the PLL (Phase Locked Loop), and has devoted a number of articles to designs incorporating this versatile circuit, as well as to explaining the principles of different applications. The Universal OTA (Operational Transconductance Amplifier) PLL described here is a printed-circuit module which can form the nucleus of many different types of receiver.
of 20 dB, the overall receiver sensitivity for the quoted audio output of 700 mV will be some 0.3 µV, which is better than that of most commercial receivers for this band.

For reception of wide-band broadcast FM signals, the unusual arrangement of a double superheterodyne, with a second IF as low as 455 kHz, is used (see figure 2). The low modulation index of a stereo FM signal makes demodulation with a good signal-to-noise ratio difficult to achieve, and even in the best (and most expensive) receivers this is seldom above 50 dB on strong signals. With this very low second IF, 60 dB is achieved.

Yet again: what is a PLL?

For those who have not yet had an opportunity to familiarise themselves with the basic concept of the phase-locked loop, the essential features of this circuit can be repeated. The key element is a voltage-controlled oscillator. When the loop is used in a receiver, this oscillator is automatically synchronised with the carrier of the incoming signal. The other elements in the loop are subservient to the main purpose of keeping the oscillator synchronised. In practice, this is done by maintaining a constant phase difference between the incoming signal and the oscillator output: hence the term 'phase-locked loop'. By definition, the oscillator is voltage-controlled. So if the incoming signal is frequency-modulated, the control voltage applied to the oscillator to keep it synchronised becomes, of itself, the demodulation of the incoming signal. As
a method of detection, this has important advantages over other methods in terms of better rejection of interfering signals, lower distortion, and better signal-to-noise ratio.

**Circuit description**

The input is fed in across resistor R1 (figure 3). The value of this resistor must be selected to give correct matching to the preceding mixer stage, and suitable values will be given in later articles describing particular applications. Transistors T1 and T2 form a differential amplifier with an asymmetrical input, while T3 and diodes D1 and D2 stabilise the current flowing through T1 and T2. The two collectors of the differential amplifier are connected through capacitors C4 and C5 to the two differential inputs (2 and 3) of the CA3080 operational transconductance amplifier IC1. The use of both inputs in this fashion gives an extra 6 dB gain without impairing stability and also facilitates the operation of the limiting diodes D3 and D4.

In addition to receiving the RF (or IF) signal at the differential inputs (pins 2 and 3), IC1 is fed via pin 5 with the output of the voltage-controlled oscillator formed by T4 and T5. Although this oscillator is described as voltage-controlled, it should more properly be called current-controlled, the current being regulated by T6 and T7 in the emitter leads of T4 and T5 respectively.

In the foregoing description the path of the loop has, in effect, been followed in the reverse direction. Recapping and going the correct way round: the DC component of the signal at pin 6 of the phase-comparator IC1 is amplified by T6 and T7 and controls the frequency of oscillator T4 + T5.

As in all FM detectors, AM rejection is important. The CA 3080 has good AM rejection at low input-signal levels, but is less good at higher levels. These higher levels, however, are taken care of by the clipping diodes D3 and D4, which begin contributing to AM rejection when the peak-to-peak signal between pins 2 and 3 of IC1 exceeds 1 volt.

Capacitor C11 is one of the components whose value influences the VCO free-running frequency (455 kHz in the broadcast FM receiver, or about 10 MHz in the narrow-band FM receiver) so its value is quoted for particular applications (see Table). When the receiver is tuned by varying the VCO frequency, as in the narrow-band FM receiver, potmeters P1 and P2 come into play. When the working IF frequency is fixed, these potmeters can be used for preset adjustment.
Figure 2. Block diagram of a double superheterodyne for stereo FM reception, with intermediate frequencies of 10.7 MHz and 455 kHz.

Figure 3. Circuit of the Universal OTA PLL.

Table: Values of R1, R14, R24, C9, C11 and C14 for specific applications.

<table>
<thead>
<tr>
<th>Mode of operation</th>
<th>Supply voltage</th>
<th>R1</th>
<th>R14</th>
<th>R24</th>
<th>C9</th>
<th>C11</th>
<th>C14</th>
</tr>
</thead>
<tbody>
<tr>
<td>(all FM)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Type of transmission</td>
<td>Intermediate frequency</td>
<td>Minimum input</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wide band mono</td>
<td>10.7 MHz</td>
<td>160</td>
<td>230</td>
<td>1 k</td>
<td>160</td>
<td>100 p</td>
<td>10 n</td>
</tr>
<tr>
<td>Narrow band</td>
<td>10.7 MHz</td>
<td>3.2</td>
<td>330</td>
<td>47 k</td>
<td>0</td>
<td>220</td>
<td>10 n</td>
</tr>
<tr>
<td>Wide band mono</td>
<td>455 kHz</td>
<td>400</td>
<td>47 k</td>
<td>2k2</td>
<td>560</td>
<td>2n2</td>
<td>10 n</td>
</tr>
<tr>
<td>Narrow band</td>
<td>455 kHz</td>
<td>20</td>
<td>3k3</td>
<td>82 k</td>
<td>560</td>
<td>2n2</td>
<td>10 n</td>
</tr>
<tr>
<td>Wide band stereo</td>
<td>455 kHz</td>
<td>500</td>
<td>47 k</td>
<td>2k2</td>
<td>220</td>
<td>2n2</td>
<td></td>
</tr>
<tr>
<td>Wide band stereo</td>
<td>455 kHz</td>
<td>200</td>
<td>47 k</td>
<td>2k2</td>
<td>220</td>
<td>2n2</td>
<td></td>
</tr>
</tbody>
</table>

* At the PLL! (— = omitted)

The low-pass filter which removes the unwanted 'sum' frequency (oscillator plus input signal) is formed by C8, C9, R14 and R16. As the values of these resistors also affect the VCO free-running frequency, they have to be selected carefully for each application. In practice, R16 is given a fixed value of 68 kΩ while R14 is specified for each application. This also applies to the feedback resistor R24 which controls the gain of the output audio amplifier T8 and T9. Resistor R28 and capacitor C14 provide de-emphasis. It will be seen that the whole of the DC component at the output (pin 6) of the phase comparator is passed to the VCO: this helps to ensure a large 'hold range' for the loop.

Detailed descriptions of applications of the Universal PLL will be given in later articles, but the two which have already been mentioned can be briefly discussed here.

Resistors:
- R1, R14, R24 = see table
- R2, R4, R11, R12, R28 = 4 kΩ
- R5, R6, R15, R17, R18, R19, R20 = 1 kΩ
- R9, R10, R23 = 10 kΩ
- R5, R6 = 560 Ω
- R7 = 100 Ω
- R27 = 100 kΩ
- R13, R22 = 220 kΩ
- R16 = 65 kΩ
- R21 = 470 kΩ
- R25, R26 = 2 kΩ
- P1 = 1 kΩ
- P2 = 100 kΩ

Capacitors:
- C1, C2, C6, C10 = 100 nF
- C3 = 470 μF/16 V
- C4, C5 = 22 nF
- C7 = 47 μF/16 V
- C8, C13 = 470 nF
- C9, C11, C14 = see table
- C12 = 47 μF/10 V
- C15 = 100 μF/6 V
- C16 = 10 μF/10 V
- L1 = 470 μH

Semiconductors:
- T1 ... T7 = BF 494
- T8 = BC 547
- T9 = BC 557

Inductor: IC1 = CA 3080
- D1 ... D6 = 1 N 414B
Narrow-band FM receiver

In narrow-band FM systems, noise always tends to be a problem because the modulation index (the ratio of the maximum deviation to the highest modulation frequency) is by definition low, but the good noise performance of a PLL demodulator goes a long way towards overcoming this handicap. The limiting sensitivity of the Universal PLL, when used in a narrow-band FM receiver, has already been stated to be $3.2 \mu V$, not counting the gain of the RF and mixer stages preceding it. With an input of $4 \mu V$ — slightly above the limiting value — the signal-to-noise ratio is $40 \, \text{dB}$.

The principle of using a crystal-controlled fixed-frequency local oscillator, and tuning the IF with the VCO, offers a very simple and effective form of band-spreadning.

Stereo FM receiver

FM sound broadcasting has a maximum deviation of $75 \, \text{kHz}$, which gives a modulation index of 5 on mono transmissions having a $15 \, \text{kHz}$ audio bandwidth. With a stereo transmission, the maximum modulation frequency is $53 \, \text{kHz}$, but the effective bandwidth of the composite stereo signal is greater than this, and in practice the modulation index works out as low as 0.6. This means that, 'other things being equal', stereo reception has a signal-to-noise ratio $20 \, \text{dB}$ lower than the same stereo transmission reproduced in mono. These problems are discussed more fully in 'Modulation Systems' (Elektor 2, p. 246 and Elektor 3, p. 454).

A PLL detector can help considerably in this situation, because it can easily be made to work on a very low second IF. The output of an FM demodulator is proportional to the quotient of the deviation and the working frequency. If, therefore, the working (intermediate) frequency is as low as $455 \, \text{kHz}$, the output will be considerably greater than with the normal intermediate frequency of $10.7 \, \text{MHz}$, while the noise will be approximately the same in both cases. In theory, a 'normal' discriminator could be made with this working frequency and the usual $75 \, \text{kHz}$ deviation, but it would be difficult to make it work satisfactorily. A PLL demodulator, on the other hand, lends itself readily to working with these parameters and enables a $60 \, \text{dB}$ signal-to-noise ratio to be obtained.

Figure 4. Printed circuit board.

Figure 5. Component layout of the universal OTA PLL.
A television pattern generator is one of the most useful TV service aids. It simplifies checking of the video stages, adjustment of picture geometry, and perhaps most important, setting up of convergence in colour receivers. Using logic IC's for the generation of the test pattern allows the construction of a simple and reliable circuit, and the design given here is based on the 74 series TTL logic family.

### Building up the video signal

The number of bars in the display has certain constraints placed upon it by the nature of the television picture. This is composed of a raster of 625 lines. Since the horizontal bars are produced by dividing down the 15625 Hz line frequency digitally, it follows that the ratio (625 : number of bars) must be a whole number, as it is not possible to obtain a non-integral division ratio digitally, and if it were the pattern would move anyway.

Since 625 = 25² then 25 is a convenient number of bars. One of these is lost during the field blanking interval, so only 24 are in fact displayed. Since the 'boxes' formed by the bars should ideally be squares rather than rectangles this determines the number of vertical bars. The aspect ratio of a television picture is 4 : 3, so the number of vertical bars is \( \frac{24 \times 4}{3} \) or 32. The oscillator which produces the vertical bars runs at a higher frequency than line frequency (since there are several picture elements along each line).

The circuit can conveniently be divided into two sections. The video generator, which produces the actual pattern, and a synchronising unit which produces the field and line sync pulses and also provides the timing for the video generator. The circuit of the video generator is given in figure 1. The vertical bar generator S1 is a NAND Schmitt trigger connected as an astable multivibrator. Since the TV line frequency is 15625 Hz and there are 32 vertical bars it follows that the frequency of this astable must be 500 kHz. P1 provides some adjustment so that the number of lines can be varied slightly. This oscillator is synchronised by line sync pulses. Each line sync pulse turns on T1, grounding pin 5 of S1 and momentarily blocking the oscillator. When the line sync pulse finishes T1 turns off and the oscillator restarts. This ensures that the pulses which make up the vertical bars occur at the same point along every line of the TV picture, as otherwise a random pattern would result.

---

**Parts list for figures 1 and 6**

**Resistors:**
- R1 = 1 k
- R2, R3 = 470Ω
- P1 = 470Ω lin.
- P2 = 1 k lin.

**Capacitors:**
- C1 = 1μF
- C2 = 220 p
- C3 = 220 n/250 V

**IC's:**
- IC1 = 7400
- IC2 = 7413
- IC3, IC4 = 7490
- IC5 = 7402
The output of the astable has substantially a 1:1 mark space ratio. This would, if used as the video signal, produce black and white vertical bands of equal thickness. However, for the purposes of the pattern generator very narrow bands provide more information about the state of the video stages of the TV, since a narrow band requires a shorter pulse length and hence a greater bandwidth.

Accordingly the output of the astable is differentiated by C2 and R3, and the spiky pulses are fed into a second Schmitt trigger to square them up again. This also inverts the signal, so it is inverted a second time by N1 to appear in the correct sense. Figure 2 shows the vertical signal V as it appears at the output of N1. The absence of pulses where the sync pulses occur can be clearly seen. The pulse length of the V signal is about 200 ns.

Line sync pulses at the collector of T1 are also counted by IC3 and IC4, which are 7490s connected as divide-by-five counters. Output D of IC4 is therefore a pulse train at 1/25 of line frequency. The timing diagram for this division is shown in figure 3. Waveform 'a' is the line sync input. Waveform 'b' is the D output of IC3, and waveform 'c' is the D output of IC4. However, this waveform cannot be used directly as the horizontal video signal, as the pulse length is equal to 5 line periods, which would make the horizontal bars too thick. For this reason it is 'NANDed' with waveform 'b' in N2 and then inverted by N3 to produce waveform 'd' (H). This has a duration of 64 \(\mu\)s or one line period. However, due to interlace each horizontal bar will actually have a thickness of two lines. Figure 4 shows an oscillogram of the H signal.

To produce the complete video signal, the H and V signals must be summed. To produce the crosshatch pattern the horizontal and vertical signals must be 'OR-d' together, as there must be a bar when vertical or horizontal pulses are present. For the dot pattern, which corresponds to the crossing points of...
Parts list for figures 5 and 7

Resistors: | Capacitors: | Semiconductors: |
---|---|---|
R1 = 270 Ω | C1 = 10 n | IC1 = 7413 |
R2 = 27 k | C2 = 820 p | IC2-IC5 = 7490 |
R3 = 18 k | C3 = 220 n | IC6 = 74123 |
R4 = 39 k | C4 = 33 n | D1 - D4 = DUS |
R5 = 10 k | | |
P1 = 1 k lin. (part of video generator) | | |
P2 = 100 $|$ preset | | |

When using this circuit as is, the pattern must appear only when horizontal and vertical bars, the pattern must appear only when horizontal and vertical information are present. The H and V signals are thus ANDed together. These functions are performed by N4 and N5 respectively, and S1 selects the pattern. N6 and S2 provide the option of a positive or negative pattern i.e. white pattern on black background or black pattern on white ground. Note that peak white corresponds to logic '0'.

Critical, and several turns of insulated connecting wire a few cm diameter should prove suitable. The video signal is then taken from P1 via C3 and is injected into the video stages of the TV. P1 adjusts the video level so that the signal does not interfere with the synchronisation of the set.

A more elegant solution is to employ a built-in sync generator, the circuit of which is given in figure 5. Again a Schmitt trigger operates as an astable multivibrator, this time at a frequency of 250 kHz. The divide-by-two stages of seven 7490's are used to divide this down to the line frequency of 15625 Hz. The 50 Hz field sync pulses are produced by taking the output of the third divide-by-two stage (31250 Hz) and feeding it back through the divide-by-five stages of the four 7490's. Since the field and line sync pulses must have pulse lengths of about 250 μs and 4 μs respectively the 50 Hz and 15625 Hz outputs are used to trigger the two halves of a 74123 dual multivibrator, with appropriate time constants.

The line sync pulses are used to trigger the video generator, and are also mixed with the field sync pulses and the video signal using the diode-resistor mixer network. Note that the output capacitor of the video generator is replaced by D4 in this circuit. The video output is taken from point B, and may be injected directly into the video stages of the TV set. Alternatively, the VHF/UHF modulator for the TV-tennis (described elsewhere in this issue) can be used.

Construction

A printed circuit board and component layout for the video generator are shown in figure 6, and for the sync generator in figure 8. Photographs of the completed boards are shown in figures 7 and 9.
Many electronics enthusiasts look on solder removing as a loathsome job. This is especially true of printed circuit boards with narrowly-spaced conductors. Things which often happen when one is trying to desolder are:

- The solder forms bridges between the conductors.
- Blobs of solder drop off the board.
- De-soldering tools or wicks are available commercially, but there is no need to lay out that kind of money. Any workshop toolbox should yield a really cheap device which will do the trick — a pencil.

Propelling pencils with long leads of 2B or B hardness are particularly suitable (e.g. clutch pencils). To remove solder from a hole, the solder must be heated with a soldering iron until it melts (figure 1). The next step is to stick the pencil point in the hole, and take away the iron (figure 2). Where the pencil point touches molten solder, the solder jumps away, because of its surface tension, and the hole is cleared of solder (figure 3).

A similar method can be used for getting rid of bridges of solder between tracks. To do this, the pencil point is laid flat on the molten solder between the tracks.
Hall effect IC

Special features of a new Mullard Hall-effect integrated circuit, type TCA450A, include: small physical size, wide operating voltage and temperature ranges, high sensitivity, low offset flux, and self balancing. It can therefore be used to advantage in the measurement of magnetic field strengths in small areas or gaps.

The function of the TCA450A is to translate information about the polarity and strength of a magnetic field into a differential output current. The device is monolithic and consists of a silicon Hall-effect element and two associated integrated amplifiers encapsulated in a miniature low profile plastic package.

Typical applications include the provision of isolated current sensing and control in high current applications, contactless and highly reliable electronic switching, sensing and control in electromagnetic systems where the field strength must be maintained at a precisely determined level, the conversion of magnetic quantities into proportional currents and the detection and positional movement of rotating shafts.

<table>
<thead>
<tr>
<th>Data</th>
<th>Min. Typ. Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>4 8 16 V</td>
</tr>
<tr>
<td>Magnetic sensitivity of Hall element</td>
<td>0.4 V/T</td>
</tr>
<tr>
<td>Voltage gain of amplifier</td>
<td>305 mA/V</td>
</tr>
<tr>
<td>Mutual conductance of amplifier</td>
<td>±240 mT</td>
</tr>
<tr>
<td>Offset flux density in balanced condition</td>
<td>±25 mT</td>
</tr>
</tbody>
</table>


C.R.T. probe attachment

A new probe attachment has been introduced by Brandenburg Limited for use with the company's direct-reading high-voltage meters. The beryllium-copper attachment which screws into the existing h.v. probe unit, is designed to be slipped beneath the anode connection on the c.r.t.

Brandenburg Limited, High Voltage Engineering Division, 929 London Road, Thornton Heath, Surrey, CR4 6JE.

New transistor for switched mode power supplies

The latest addition to the Mullard range of transistors for high-frequency switched mode power supplies operating direct from 'rectified mains' inputs is type BUX82. It is intended for use in 400 W push-pull or 100 W to 200 W single-ended circuits. Together with other types in the same series, the BUX82 will not only operate satisfactorily at the 'rectified mains' level, but will also accommodate the ±10% voltage variations regularly experienced on mains supplies.

To meet these requirements, the device has an open base collector-emitter rating of 400 V and a collector breakdown rating of 800 V (VBE = 0). The d.c. and peak collector current ratings are 5 A and 8 A respectively.

Fast switching characteristics not only minimize switching losses, but also facilitate high-frequency (25 kHz to 50 kHz) operation.

Range of Coiled Cables Available from Lemo

Lemo (UK) can now supply a range of coiled cables, terminated or unterminated. Up to five conductors can be ordered, in a variety of uncoiled (maximum) lengths, and these can be either telecommunications light-current varieties or with mains-carrying flexibles or with mains-carrying flex in the cores. Outer insulation can be either p.v.c. or rubber, with the conductor insulation following suit.

Lemo (UK) Ltd, 6 South Street, Worthing, Sussex BN11 3AE.

M-Tron industries establishes international division

M-Tron Industries of Yankton, South Dakota, has formed an International Division to sell their crystals to the overseas market. The new international division will be located at 2200 Shames Drive, Westbury, L.I., New York 11150. Telex 961474.

M-Tron Industries manufacture a wide line of quartz crystals. Producing over 10 million crystals a year, they are the number one manufacturer of CB and monitor crystals in the United States.

Combined C-MOS and bipolar relay driver package

The MM74C908/918 Dual High Voltage C-MOS driver consists of two C-MOS "NAND" gates driving a bi-polar emitter-follower Darlington to achieve high current drive and high voltage capabilities, while having the very low input-current characteristics of complementary-metal-oxide. The MM74C908/918 specifications are at a min. 30 V breakdown voltage and an output current range between 250 mA and 350 mA. However, this component is aimed at the telecommunications market and was specifically designed to replace high voltage telephone relay drivers. Therefore, an improved version for this usage will be specified at 56 V min., packaged in a 14-lead, 2.5 Watt configuration.

The main advantage of this new C-MOS High Voltage Driver is its nil power consumption - just leakage current in the stand-by-mode, while a conventional telephone relay driver in the same mode uses about 10 to 20 mA. The dual high-voltage C-MOS drivers will be available in two different versions, the MM74C908N 8-pin moulded dual-in-line package and the MM74C918N 16-pin moulded dual-in-line package.

National Semiconductor, The Precinct, Broxbourne, Herts. EN10 7HY.

'Switchmode' power transistors

Motorola have just introduced the switchmode series of power transistors. Designed for high-voltage power switching applications, the first devices in this series are designated 2N6542 to 2N6547 and are n-p-n triple-diffused silicon transistors. Before these devices were introduced, designers of power equipment had to use transistors that were often only specified for resistive loads at room temperature. Unfortunately, in real life things are seldom so simple and, consequently, the designer was often faced with the task of using power devices at high temperatures and with reactive loads without sufficient information as to how the transistors were likely to perform under these conditions.

Featuring in the data sheets for these devices are all the significant specifications for high temperature use (TC = 100°C) and for secondary breakdown under base forward-biased and base-reverse-biased conditions. Dynamic voltage capabilities (sustaining voltages) are given for VCEO (SUS) and VCEX (SUS). Furthermore, VCEO (SUS) minimum is specified at two values of IC at a case temperature of 100°C, with the device driving a clamped inductive load. A blocking voltage rating, VCEV, is specified at the same case temperature and maximum values for VCE (sat)-VBE (sat)-ICER and VqEx are also provided.

Fall time and storage time, important parameters for switching performance, are specified at rated IC, VCE (SUS) and TO = 100°C, with an inductive load.

CHARACTERISTICS OF NEW SWITCHMODE POWER TRANSISTORS

<table>
<thead>
<tr>
<th>VCEX @TC = +100°C</th>
<th>VCEV</th>
<th>VCEO</th>
<th>VCE (SAT) @TC = +100°C</th>
<th>VBE (SAT) @TC = +100°C</th>
<th>Ic peak (Amps)</th>
<th>Ic continuous (Amps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>350 V</td>
<td>650 V</td>
<td>300 V</td>
<td>2 V</td>
<td>1.4 V</td>
<td>10</td>
<td>5</td>
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CHARACTERISTICS OF NEW SWITCHMODE POWER TRANSISTORS

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<td>2 mj</td>
<td>125 µJ</td>
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New Mains Filters for Electrical Equipment

Tekdata announce the availability in U.K. of a new mains filter incorporating an I.E.C. socket. The units are Underwriters Laboratories approved and are designed in accordance with the I.E.C., V.D.E., C.S.A. and the proposed American Standards Association specifications.

Each filter measures only 40.6 mm square by 20.5 mm high, and is incorporated in the panel-mounted recessed connector on the equipment. Current ratings from 1 to 6 amps, are available, for voltages of 125/250 at 0 to 60 Hz. Equipment connection to the mains input/filter combination is by solder lugs. Maximum leakage to earth is 0.25 mA at 125 V, and 0.5 mA at 250 V; the filters will withstand a dielectric test of 2,100 V d.c.

Tekdata Ltd, Westport Lake, Canal Lane, Tunstall, Stoke on Trent, Staffs. ST6 4PA.

Heat sinks

The range of heat sinks produced by Dieter Assmann Electronics Limited now includes extruded metal, die cast staggered finger and spring types. More than 35 different versions of standard extruded metal heat sinks are stocked. The total range of standard products, which includes more than 80 heat sinks of a variety of shapes and dimensions, is one of the most comprehensive available from a single source.

Dieter Assmann Electronics Ltd, Victoria Works, Water Lane, Watford, Herts. WD1 2NW.
In connection with the rapid growth of Elektor, we are now looking for an assistant editor.

Applicants should have a sound knowledge of electronics and an ability to write lucidly on that subject. Previous journalistic experience is not essential but would be an advantage, as would a knowledge of the German language.

The successful applicant will have the opportunity to assist in the technical development of our magazine. Conditions of employment: attractive salary, 37½ hour week, 8.3% holiday bonus and 3.5% Christmas bonus, etc.

Applications with career details should be addressed to the Managing Director, Elektor Publishers Ltd, 6 Stour Street, Canterbury CT1 2XZ.

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**PLASTIC BOXES**

Two new ranges of ABS plastic boxes are offered at competitive prices and with short deliveries. The first range, for electronic circuits and controls, gives volumes from 348 to 1,369 cc in four sizes.

The second, for potting, gives 41 to 187 cc in three sizes. ABS material is said to be antistatic, easily punched and drilled, and capable of withstanding 100°C. Standard colours offered are grey, blue, orange and red.

**Albol Ltd.**


---

**MISSING LINK**

The most recent experiments with the TAP-power (this issue, page 1130) have shown that the most reliable circuit for the touch inputs is as follows:

- capacitors $C_a$ and $C_d$ are included across the touch contacts, $C_b$ and $C_c$ are omitted;
- the connections from the touch panels to the main pcb are made via 1 MΩ series resistors instead of wire links, e.g. a 1 MΩ resistor connects the junction of the 'ON' touch panel and $C_a$ to the junction of $R_{20}$ and pin 8 of $N_1$. 

---
Mercury-wetted relays

From Astralux Dynamics Limited, the 270/280 series of miniature mercury-wetted reed relays are ideal for low-level switching applications. The mercury wetting of the relay contacts eliminates electrical contact 'bounce' and gives a stable contact resistance (initial contact rating 0.05 £1 maximum).

The avoidance of spurious operation means that the devices are suitable for interfacing with low-level logic equipment, while the relatively high power ratings enable the relays to be used for switching inductive loads. The life expectancy is also increased: up to 50 x 10^6 operations.

The relays are available in I Form A, 2 Form A, 1 Form C and 2 Form C configurations.

Ratings for the Form A types are: sneakdown 1.2 kV d.c. minimum; withstanding 200 V, 1 mA and 28 V, 1 A (1 kV d.c. and 2 A d.c. maximum); d.c. contact rating 50 W maximum.

The corresponding figures for the Form C types are: sneakdown 1 kV d.c. minimum; withstanding 200 V, 1 mA and 28 V, 1 A (200 V d.c. and 1 A d.c. maximum); d.c. contact rating 14 W maximum.

Astralux Dynamics Limited, Brightlingsea, Colchester, Essex, CO7 6SW.

P.C.B. Transfer System

This system, from J.H. Equipment Ltd allows the production of high-quality one-off printed circuits without recourse to photography. The etch-resistant pads and tracks are laid out on the copper side of the board and the resulting circuit can then be etched. The manufacturers claim that their method of applying the adhesive to the symbols gives better definition than similar systems, as there is no adhesive overlap which can produce ragged edges.

The system is available in kits of ten sheets of symbols as illustrated.

Metallised plastic film capacitors

Designated Type MKM, these capacitors are the latest in a series developed by Siemens and feature exceptional compactness, stability, low loss and close tolerance. They have been introduced principally for use in completely automated production systems but, in a protected version, are also well suited to applications in both professional and semi-professional electronic equipment.

Individual capacitors are cut from a large 'mother' capacitor of the MKM type. This is not possible when produced individually. Currently, LST Electronic Components stock the B32551 version of the MKM capacitor. This is available at voltage ratings of 100 V d.c. and preferred values of 10 to 68 nF, and at 250 V d.c. and preferred values of 100, 150 and 220 nF. The pin spacing of the B32551 is 10 mm.

LST Electronic Component Ltd, Victoria Road, Chelmsford, Essex.

Inexpensive Programmable Op-Amp

A single external resistor allows the characteristics of a new Motorola opamp to be optimised to suit power supplies from ±6 to ±15 V. Parameters which are programmed by the external resistor include input current and voltage, power consumption and current noise. The new op-amp, designated type MC3476, does not require frequency compensation, has offset null capability and is fully protected against damage from short circuits. A typical power consumption of only 4.8 mW makes the MC3476 a good choice for use in battery powered equipment.

The data sheet gives the typical offset voltage, offset current and bias current as ±2 mV, ±2 nA and 15 nA respectively. Input resistance and capacitance are 5 MΩ and 2 pF, while input common-mode voltage range, common-mode rejection ratio and supply voltage rejection ratios are quoted as ±10 V, 70 dB and 25 μV/V respectively. The output resistance is 1 kΩ and the output current into a short circuit is typically 12 mA.

From the performance point of view the MC3476 offers a minimum large signal voltage gain of 50 kV/V (min) with a 10 kΩ load and an output voltage swing of ±10 V at 25°C. Slew rate with the same load is 0.8 V/μsec and the unity gain transient response is typically 0.35 μsec.

Motorola Ltd, Semiconductor Products Division, York House Empire Way, Wembley, Middlesex.
PO BOX 6 WARE HERTS

QUALITY TESTED PAKS

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<tr>
<th>Pak No.</th>
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<td>AC 128/129</td>
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<td>AC 128/129</td>
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